# Uni-directional ESD Protection Diode

## DESCRIPTIONS

The TESDA6V0U40P1Q0 is a Unidirectional ESD rated clamping cell to protect power interfaces, or one control line, or one low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

ESD protection device in an ultra-small DFN0603 Surface-Mounted Device (SMD) plastic package designed to protect two automotive In-vehicle network bus lines from the damage caused by Electrostatics discharge (ESD) and other transients.

The TESDA6V0U40P1Q0 may be used to provide ESD protection up to ±30kV (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 5A (8/20µs) according to IEC61000-4-5.

## FEATURES

- AEC-Q101 qualified
- Provide ESD protection to
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 5A (8/20us)
- Suitable for 6V and below, operating voltage applications
- Ultra small packages save board space
- Protect one I/O line or one power line
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free

## APPLICATION

- Portable medical devices
- Smart phones
- PDAs

| PACKAGE: DFN0603-2L | PIN CONFIGURATION | CIRCUIT DIAGRAM |
|:---:|:---:|:---:|
|  |  |  |
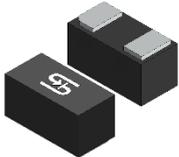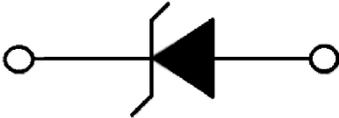
## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Typical peak pulse power (tp = 8/20us) | $P_{PK}$ | 48.5 | W |
| Peak pulse current (tp = 8/20us) | $I_{PP}$ | 5 | A |
| ESD according to IEC61000-4-2 air discharge | $V_{ESD}$ | ±30 | kV |
| ESD according to IEC61000-4-2 contact discharge | | ±30 | kV |
| Operating junction temperature range | $T_J$ | -55 to +150 | °C |
| Storage temperature range | $T_{STG}$ | -55 to +150 | °C |

## ELECTRICAL SPECIFICATIONS ($T_A$ = 25°C unless otherwise noted)

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Reverse working voltage | | $V_{RWM}$ | - | - | 6 | V |
| Reverse breakdown voltage | $I_R$ = 1mA, $T_J$ = 25°C | $V_{BR}$ | - | 7.5 | - | V |
| Forword voltage | $I_F$ = 1mA, $T_J$ = 25°C | $V_F$ | - | 0.76 | - | V |
| Reverse leakage current | $V_{RWM}$ = 6V, $T_J$ = 25°C | $I_R$ | - | 37.3 | 500 | nA |
| Clamping voltage[1] | $I_{PP}$ = 1A, tp = 8/20us | $V_C$ | - | 7.9 | - | V |
| | $I_{PP}$ = 2A, tp = 8/20us | | - | 8.4 | - | V |
| | $I_{PP}$ = 5A, tp = 8/20us | | - | 9.7 | - | V |
| Clamping voltage[2] | $I_{TLP}$ = 4A, tp = 100ns | $V_{CL}$ | - | 8.9 | - | V |
| | $I_{TLP}$ = 16A, tp = 100ns | | - | 12.7 | - | V |
| Junction capacitance | 1MHz, $V_R$ = 0V | $C_J$ | - | 36.5 | 40 | pF |
| | 1MHz, $V_R$ = 2.5V | | - | 20.6 | - | pF |
| Dynamic resistance[2] | | $R_{DYN}$ | - | 0.32 | - | Ω |

**Notes:**

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: $Z_0$ = 50 Ω, tp = 100ns, tr = 2ns, averaging window from 60ns to 80ns. $R_{DYN}$ is calculated from 4A to 16A.

## ORDERING INFORMATION

| ORDERING CODE | PACKAGE | PACKING |
|---|---|---|
| TESDA6V0U40P1Q0 M6G | DFN0603-2L | 15,000 / 7" Reel |

# CHARACTERISTICS CURVES

($T_A$ = 25°C unless otherwise noted)

**Fig.1 Peak Pulse Power vs. Junction Temperature**  **Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time**
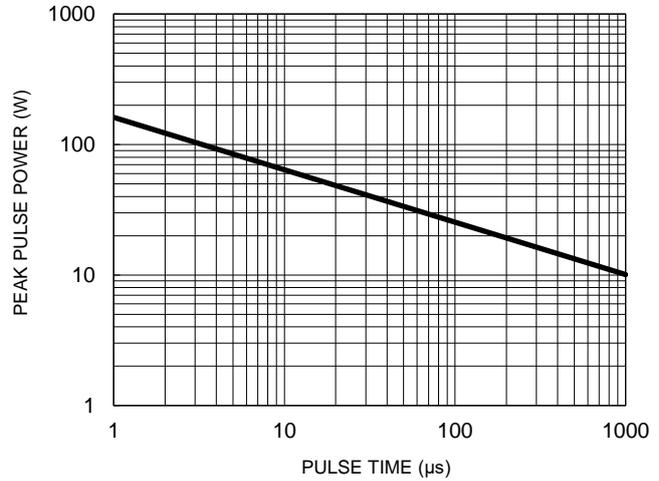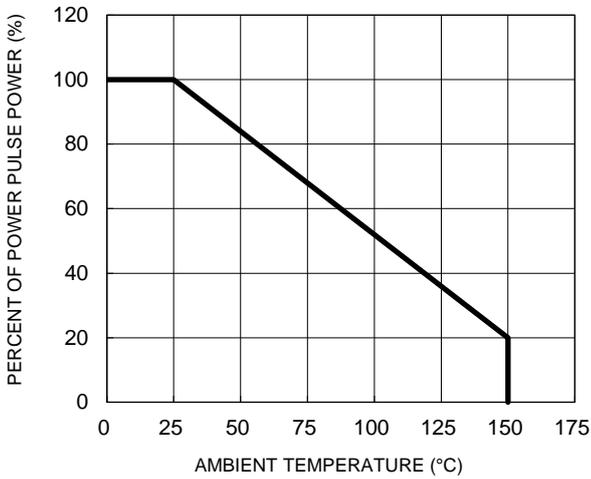
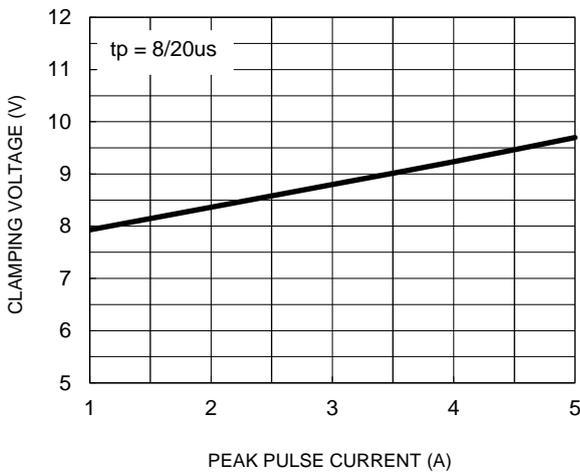**Fig.3 Clamping Voltage vs. Peak Pulse Current**  **Fig.4 Capacitance vs. Reverse Voltage**
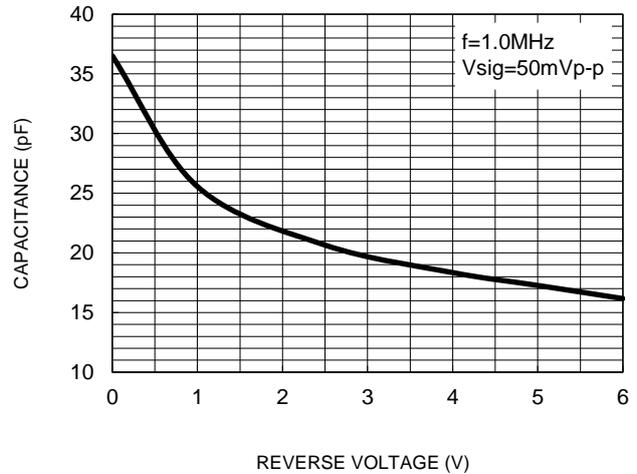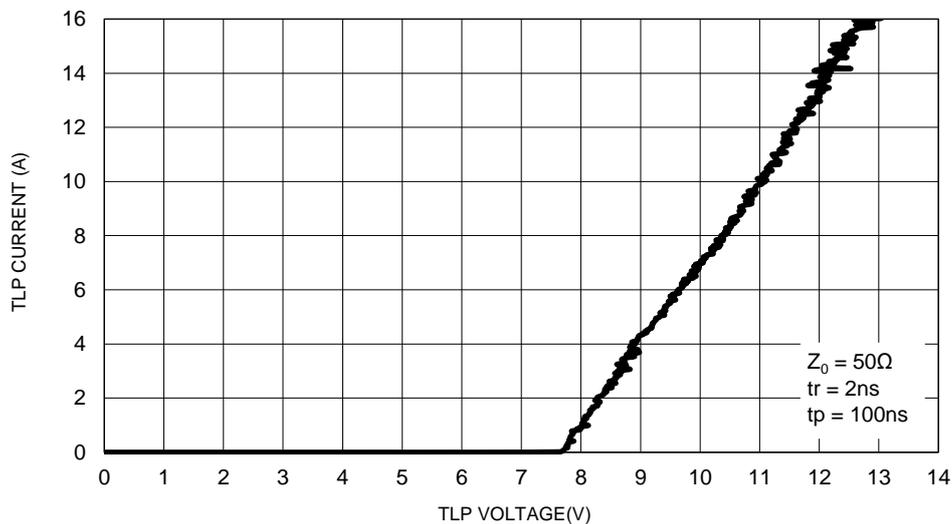
**Fig.5 TLP Curve**

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# CHARACTERISTICS CURVES

($T_A$ = 25°C unless otherwise noted)

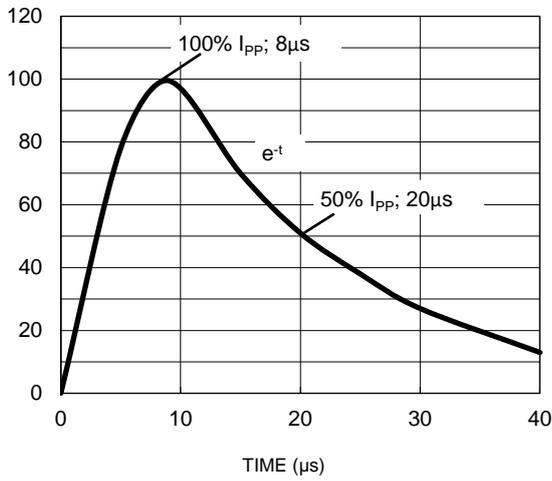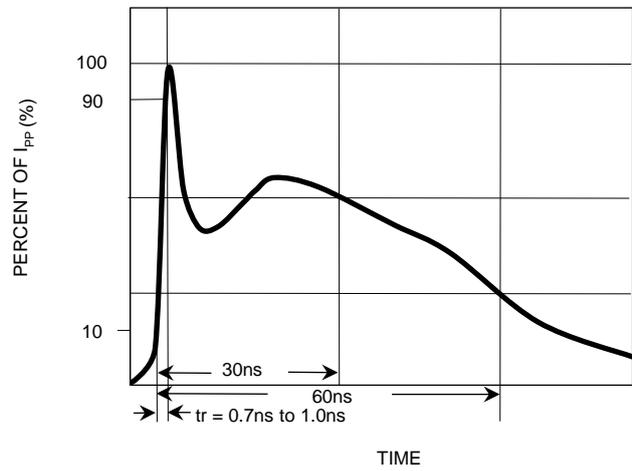**Fig.6 8/20µs pulse waveform per IEC61000-4-5**

**Fig.7 ESD pulse waveform per IEC61000-4-2**

## APPLICATION INFORMATION

### Device Connection

The TESDA6V0U40P1Q0 is designed for protection from the damage caused by ESD and surge pulses.
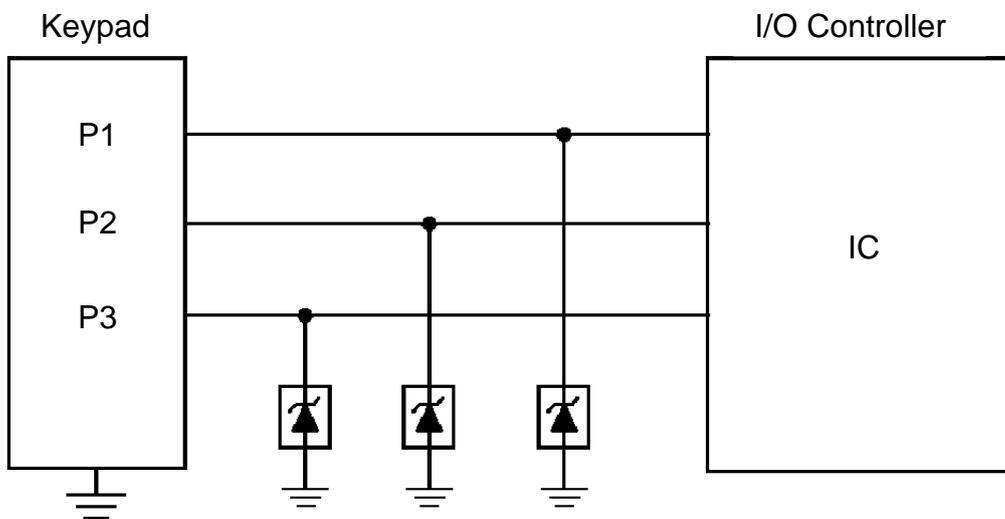The usage of the TESDA6V0U40P1Q0 is shown in Fig1.Protected line.
To minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDA6V0U40P1Q0 should be kept as short as possible.

To obtain enough suppression of ESD transient, a good circuit board is critical.    Thus, the following guidelines are recommended:
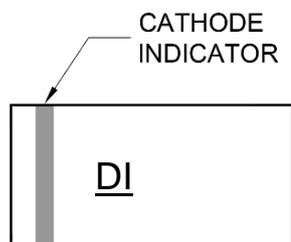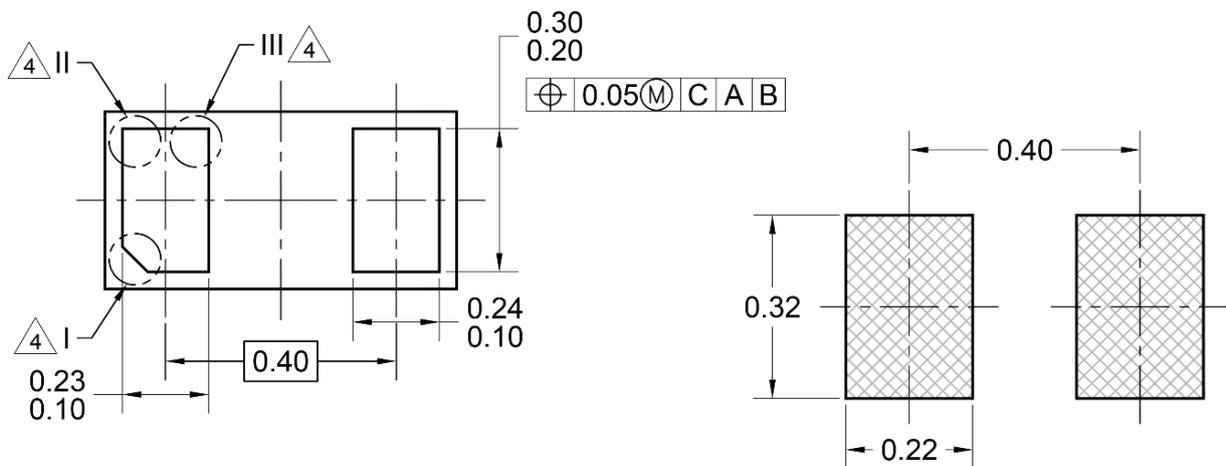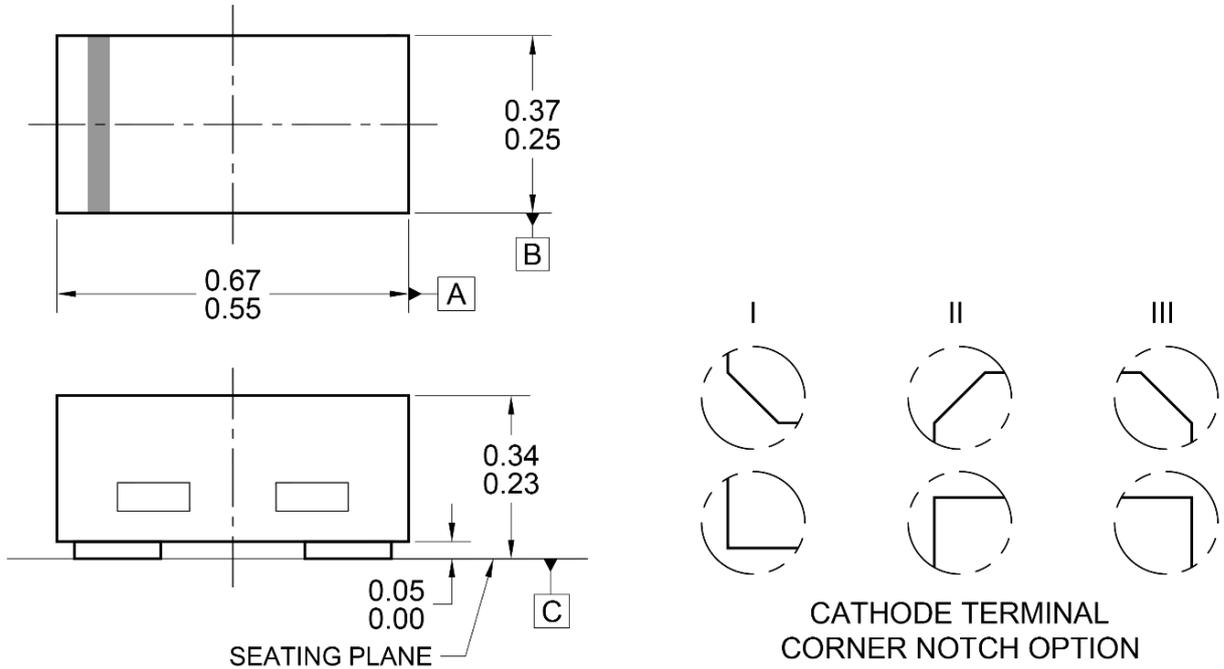
- Let the path length between the protected lines and the TESDA6V0U40P1Q0 minimize.
- Place the TESDA6V0U40P1Q0 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground plane whenever possible.

**Fig.1 ESD protection by TESDA6V0U40P1Q0**

## PACKAGE OUTLINE DIMENSIONS

### DFN0603-2L

0.37
0.25

B

0.67
0.55

A

0.34
0.23

0.05
0.00

C

SEATING PLANE

I    II    III

CATHODE TERMINAL
CORNER NOTCH OPTION

0.30
0.20

⊕ 0.05Ⓜ C A B

II

III

I

0.24
0.10

0.40

0.23
0.10

0.40

0.32

0.22

SUGGESTED PAD
LAYOUT

CATHODE
INDICATOR

DI

MARKING DIAGRAM

DI = Device Code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE SIZE CODE REFERENCE:
   EIA (inch) NAME: 0201 (0.024in x 0.012in)
   IEC (metric) NAME: 0603 (0.6mm x0.3mm)
4. CATHODE TERMINAL MAY HAVE CHAMFER NOTCH OR FULL 90 DEGREES CORNER.
5. DWG NO. REF: HQ2SD07-DFN0603-067 REV C.

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