

IRF8010PbF

SMPS MOSFET

HEXFET® Power MOSFET

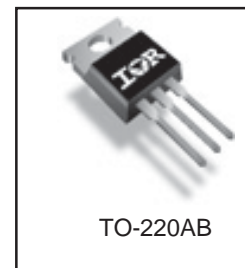
Applications

- High frequency DC-DC converters
- UPS and Motor Control
- Lead-Free

V_{DSS}	R_{DS(on)} max	I_D
100V	15mΩ	80A[Ⓞ]

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current
- Typical R_{DS(on)} = 12mΩ



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	80 [Ⓞ]	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	57	
I _{DM}	Pulsed Drain Current [Ⓛ]	320	
P _D @ T _C = 25°C	Power Dissipation	260	W
	Linear Derating Factor	1.8	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt [Ⓜ]	16	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lb•in)

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.57	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient	—	62	

Notes [Ⓛ] through [Ⓞ] are on page 8

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	12	15	m Ω	$V_{GS} = 10V, I_D = 45A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	82	—	—	V	$V_{DS} = 25V, I_D = 45A$
Q_g	Total Gate Charge	—	81	120	nC	$I_D = 80A$
Q_{gs}	Gate-to-Source Charge	—	22	—		$V_{DS} = 80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	26	—		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 50V$
t_r	Rise Time	—	130	—		$I_D = 80A$
$t_{d(off)}$	Turn-Off Delay Time	—	61	—		$R_G = 39\Omega$
t_f	Fall Time	—	120	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	3830	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	480	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	59	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	3830	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	280	—		$V_{GS} = 0V, V_{DS} = 80V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	530	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ③

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②⑥	—	310	mJ
I_{AR}	Avalanche Current ①	—	45	A
E_{AR}	Repetitive Avalanche Energy ①	—	26	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	80	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	320		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 80A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	99	150	ns	$T_J = 150^\circ\text{C}, I_F = 80A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	460	700	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

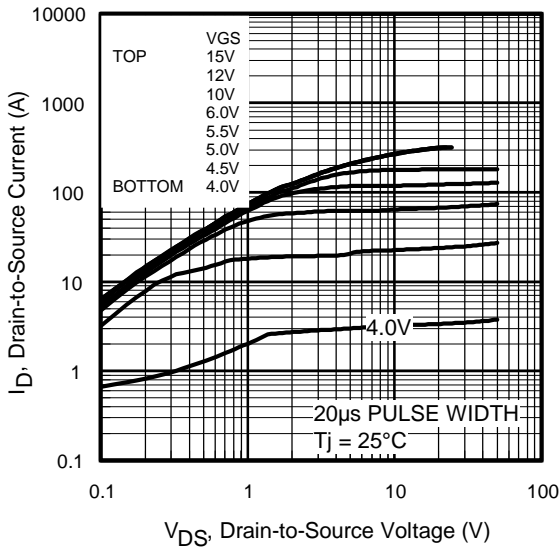


Fig 1. Typical Output Characteristics

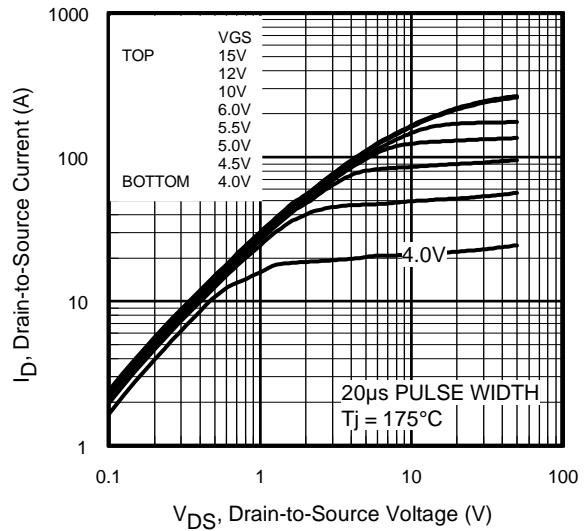


Fig 2. Typical Output Characteristics

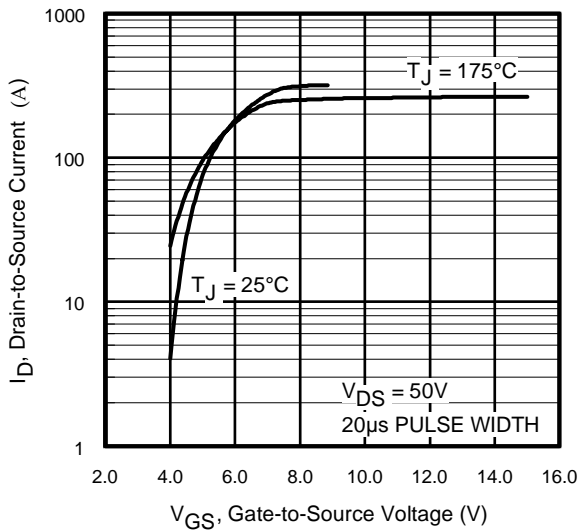


Fig 3. Typical Transfer Characteristics

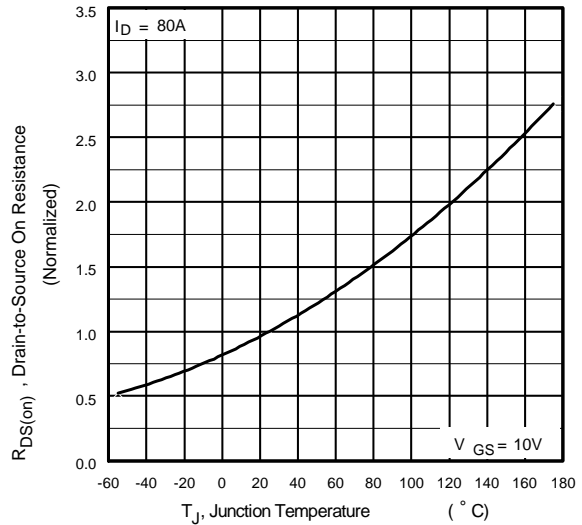


Fig 4. Normalized On-Resistance Vs. Temperature

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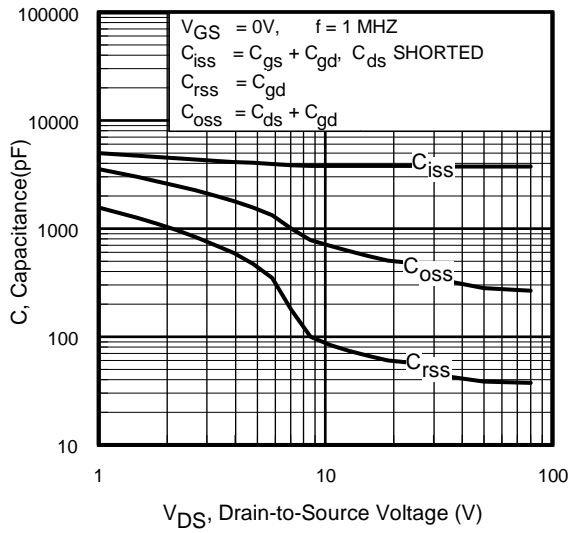


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

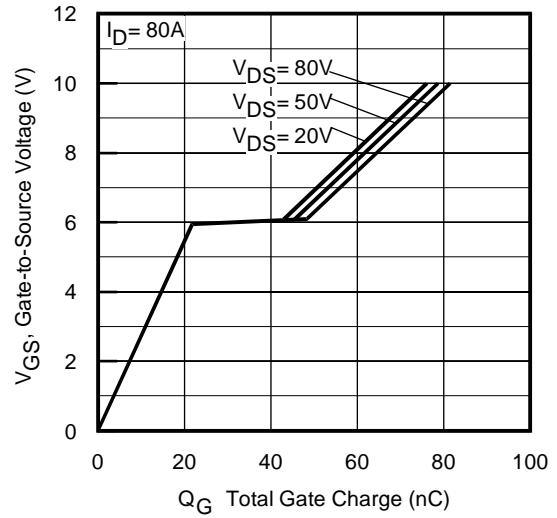


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

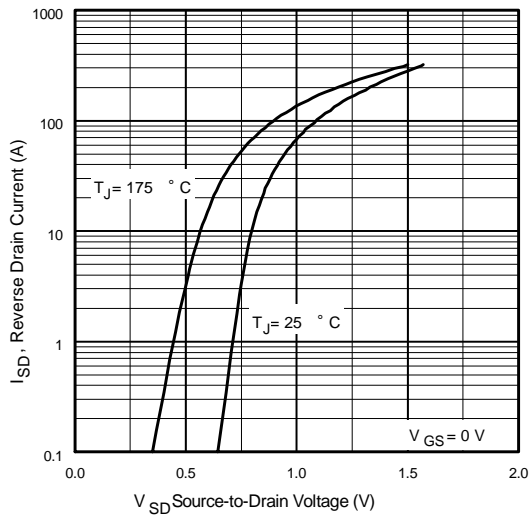


Fig 7. Typical Source-Drain Diode Forward Voltage

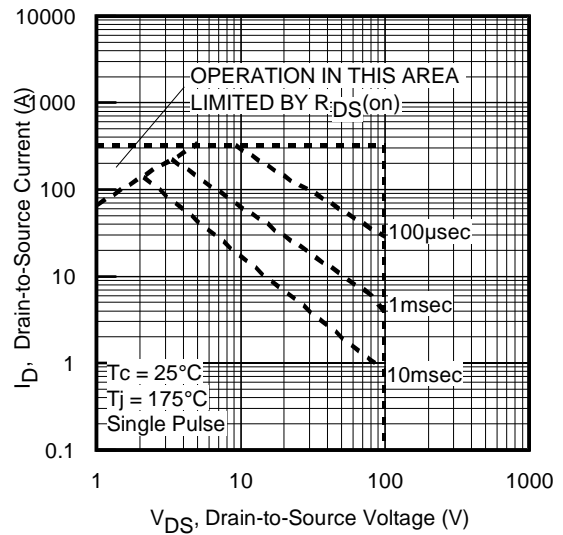


Fig 8. Maximum Safe Operating Area

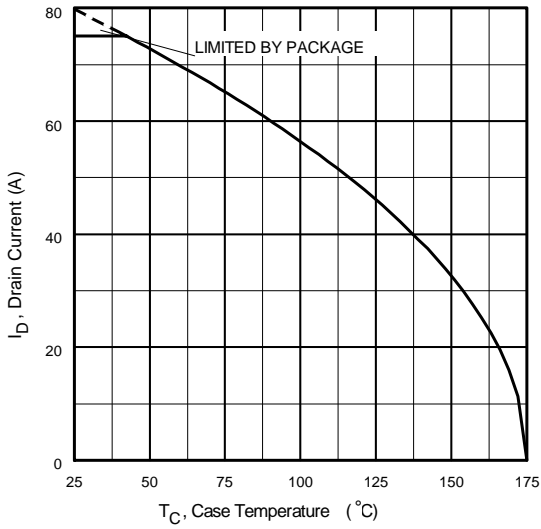


Fig 9. Maximum Drain Current Vs. Case Temperature

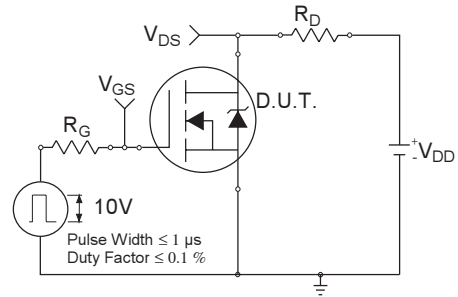


Fig 10a. Switching Time Test Circuit

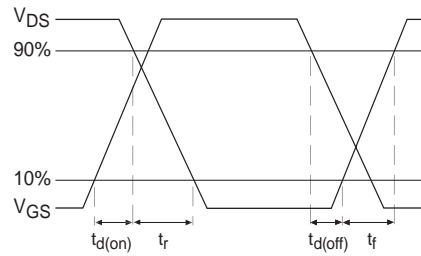


Fig 10b. Switching Time Waveforms

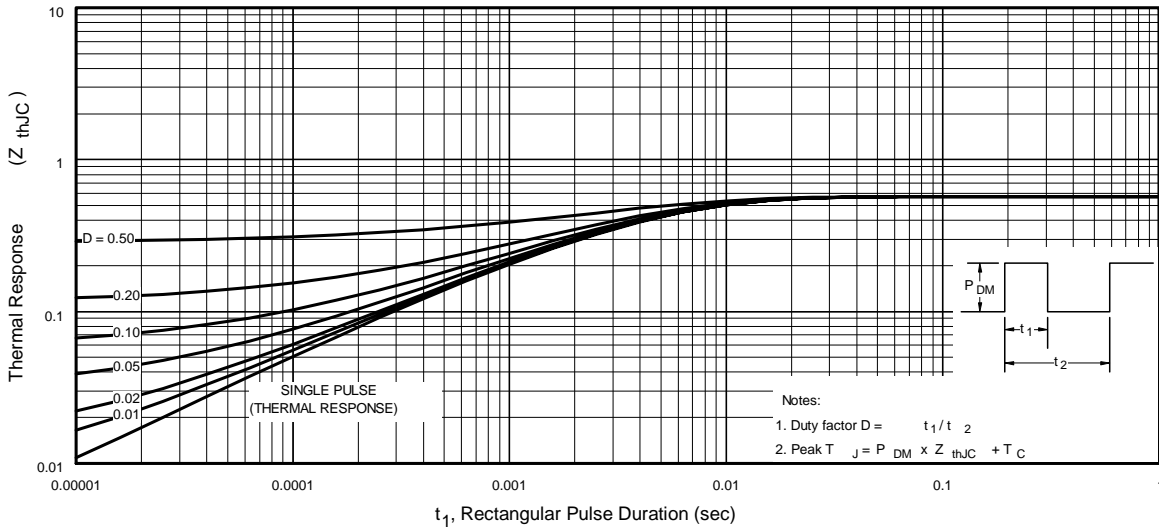


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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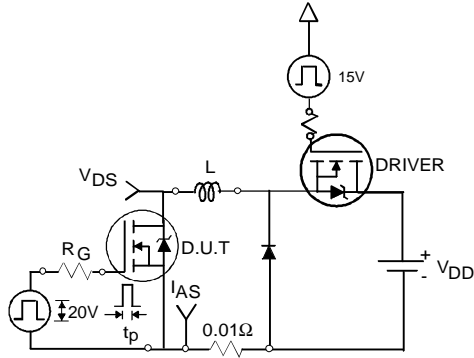


Fig 12a. Unclamped Inductive Test Circuit

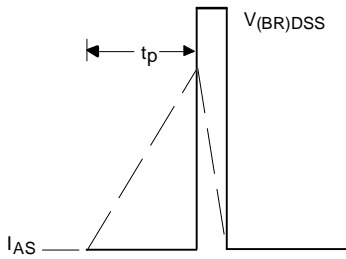


Fig 12b. Unclamped Inductive Waveforms

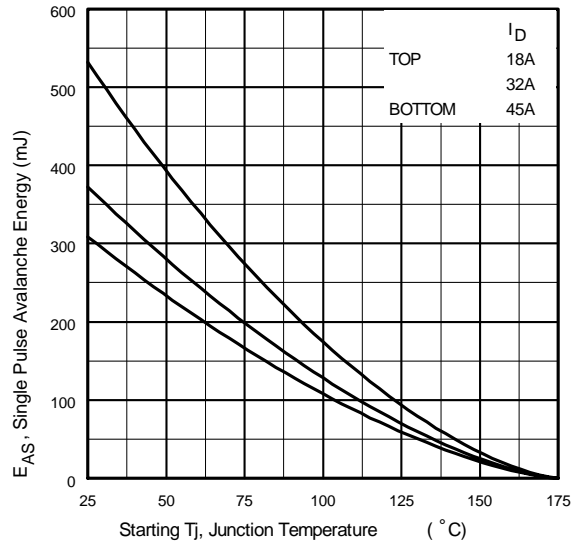


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

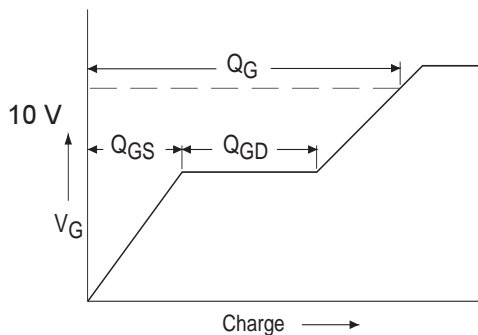


Fig 13a. Basic Gate Charge Waveform

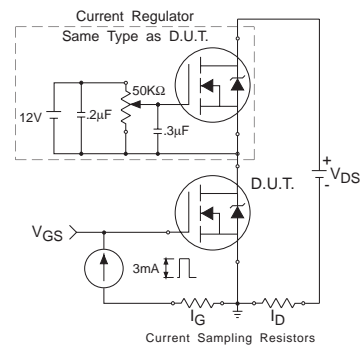


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

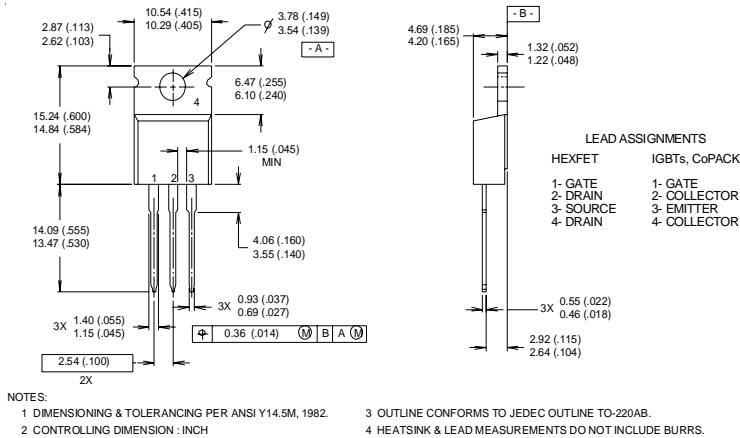
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

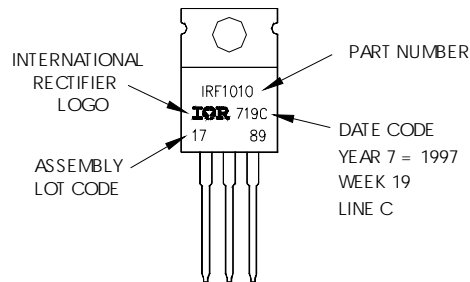
Dimensions are shown in millimeters (inches)

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TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line position indicates "Lead-Free"



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.31\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 45\text{A}$.
- ③ $I_{SD} \leq 45\text{A}$, $di/dt \leq 110\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

TO-220 package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

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<http://www.irf.com/package/>

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